LeddarTech®

DATA SHEET

LCA2 LeddarCore

2D/3D LiDAR Data Acquisition and Processing IC

Description

The LCA2 LeddarCore™ data acquisition and processing integrated circuit (IC) is the central hardware component of LeddarTech's automotive LiDAR platform.

The LCA2 LeddarCore is a multi-channel LiDAR front-end for objects detection in advanced driver assistance systems (ADAS), autonomous driving (AD), or other applications. The LCA2 LeddarEngine™ uses the time-of-flight principle of light pulses reflected by one or more objects to measure the distance between the LiDAR and objects.

A timing module is integrated in the LeddarCore to send out pulses to control the light emission and to synchronize the device to its environment. Each detection also includes a timestamp.

Each LCA2 LeddarCore has 32 parallel light acquisition channels (PD1 to PD32) that amplify, sample, and process the reflected light pulses, converted by photodetectors.

The "Sync" feature allows operations of two LCA2 LeddarCore ICs in primary/secondary mode to increase the resolution to 64 parallel light acquisition channels. Additional LCA2 ICs can be added to the system to reach the required number of channels.

A 50 MHz quad SPI interface transmits the preprocessed ADC measurements to a microcontroller (also denoted host MCU) for post-processing and calculating a 2D or 3D picture of the objects around.

Functional safety (FuSa) hardware features ensure a stable operation and fast error detection within the LiDAR system.

IC Features

- 2D/3D solid-state LiDARs front-end for object detection in advanced driver assistance systems (ADAS) and autonomous driving (AD) applications.
- 32 light acquisition channels with integrated trans-impedance amplifiers (TIA) and analog-to-digital converters (ADC).
- Single and dual mode:
  - Single-mode detection allows up to 32 light acquisition channels.
  - Dual-mode detection (Sync feature) using two LCA2 LeddarCore ICs as primary/secondary allows up to 64 light acquisition channels, while sharing the same light emitters.
- Integrated functional safety features developed for ASIL–B according to ISO 26262.
- –40 °C to +105 °C ambient temperature range
- 10 x 10 mm, 72-pin QFN package with EPAD for heat dissipation
- AEC-Q100 qualified

Typical 32 x 8 System Block Diagram

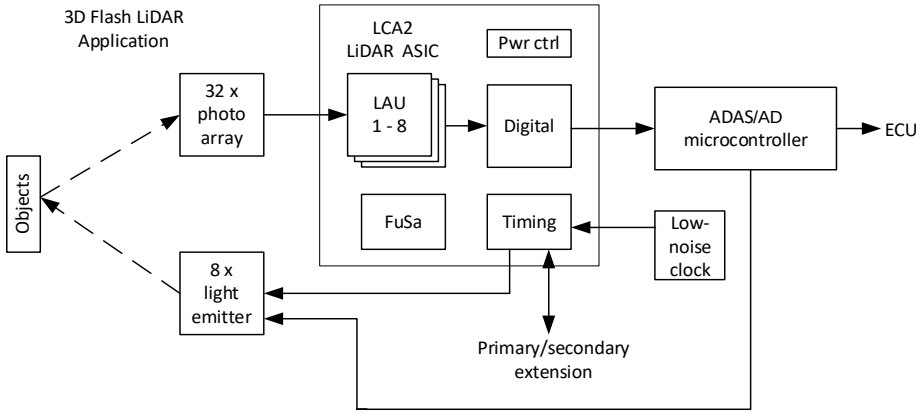

Figure 1 – Block diagram

Table of Contents

1. Glossary

Acronym	Description
AD	Autonomous driving
ADAS	Advanced driver assistance system
ADC	Analog-to-digital converter
BIST	Built-in self-test
CPHA	Clock phase
CPOL	Clock polarity
CRC	Cyclic redundancy check
EPAD	Exposed pad
FuSa	Functional safety
GND	Ground
IC	Integrated circuit
IRQN	Interrupt (active low)
JTAG	Standardized test interface (Joint Test Action Group)
LAU	Light acquisition unit
LED	Light-emitting diode
LiDAR	Light detection and ranging
LPS	Laser power supply
MCLK	Monitor clock
MCU	Microcontroller unit
NVM	Non-volatile memory
PD	Photodiode
PDPS	Photodiode power supply
PLL	Phase-locked loop
PWM	Pulse width modulation
QFN	Quad flat no-lead (package)
QSPI	Quad serial peripheral interface
RCLK	Reference clock
RSTN	Reset (active low)
SPI	Serial peripheral interface
TIA	Trans-impedance amplifier
T&H BUF	Buffered Track and Hold
ToF	Time-of-flight

2. LCA2 LeddarCore IC Block Diagram

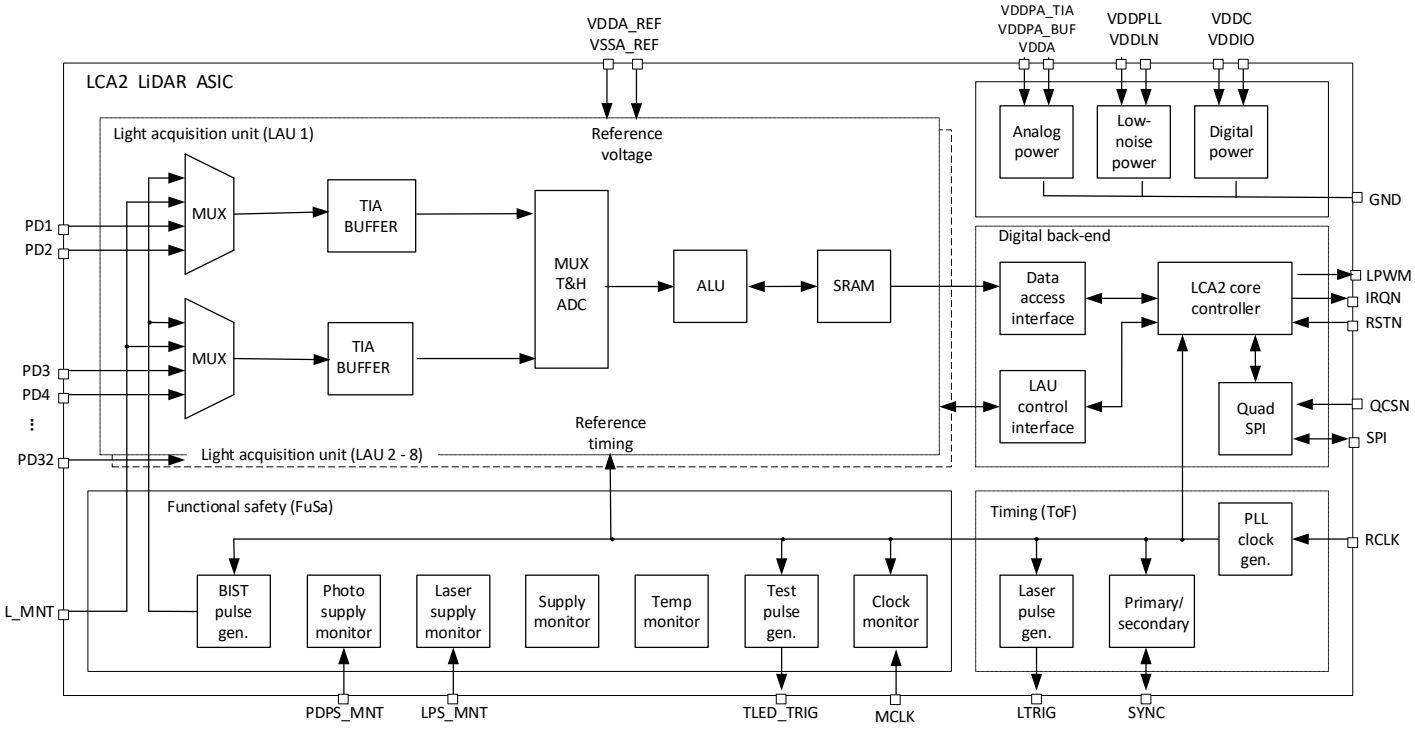

Figure 2 – LCA2 LeddarCore IC block diagram

3. Pin Assignment and Description

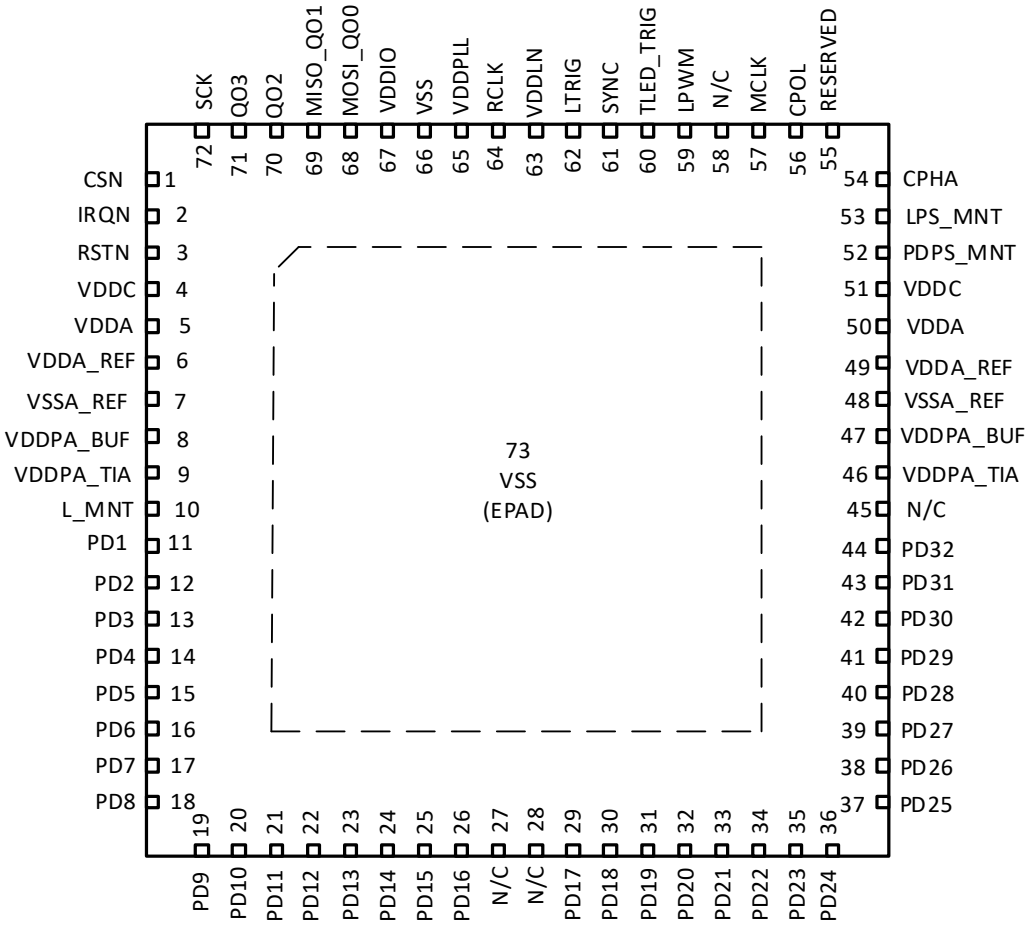

Figure 3 – Pin assignments for 10 x 10 mm QFN-72 package with 6.5 mm EPAD – top view

Table 1 – Pin description

Pin No.	Pin Name	I/O	I/O Type	Power Domain	Description
1	CSN	Input	Digital	VDDIO	SPI chip select, active low. The SPI interface is set to "High-Z" when the device is not selected.
2	IRQN	Output	Digital	VDDIO	Interrupt open drain output, active low[a]
3	RSTN	Input	Digital	VDDIO	Reset input, active low
4	VDDC	Supply	Power	VDDC	Digital core supply, 1.2 V
5	VDDA	Supply	Power	VDDA	Analog ADC supply, 1.2 V
6	VDDA_REF	Supply	Reference	VREF	Analog reference supply, 1.2 V
7	VSSA_REF	Supply	Reference	VREF	Analog reference GND
8	VDDPA_BUF	Supply	Power	VDDPA	Analog supply T&H, 2.5 V
9	VDDPA_TIA	Supply	Power	VDDPA	Analog supply TIA, 2.5 V

[a] To supply the open drain network for IRQN, an external 10 kΩ ± 10% pull-up resistor is required.

Pin No.	Pin Name	I/O	I/O Type	Power Domain	Description
10	L_MNT	Input	Analog	VDDPA	Laser monitor photodiode
11-26	PD1-PD16	Input	Analog	VDDPA	Common cathode photodiode 1-16 inputs
27	N/C	N/A	N/A	N/A	Not used in application, no termination required
28	N/C	N/A	N/A	N/A	Not used in application, no termination required
29-44	PD17-PD32	Input	Analog	VDDPA	Photodiode 17-32 inputs
45	N/C	N/A	N/A	N/A	Not used in application, no termination required
46	VDDPA_TIA	Supply	Power	VDDPA	Analog supply TIA, 2.5 V
47	VDDPA_BUF	Supply	Power	VDDPA	Analog supply T&H, 2.5 V
48	VSSA_REF	Supply	Reference	VREF	Analog reference GND
49	VDDA_REF	Supply	Reference	VREF	Analog reference supply, 1.2 V
50	VDDA	Supply	Power	VDDA	Analog ADC supply, 1.2 V
51	VDDC	Supply	Power	VDDC	Digital core supply, 1.2 V
52	PDPS_MNT	Input	Analog	VDDLN	Photodiode power supply monitor voltage
53	LPS_MNT	Input	Analog	VDDLN	Laser power supply monitor voltage
54	CPHA	Input	Digital	VDDLN	CPHA mode selection for SPI, read at power-up. Terminate with pull-up or pull-down[b].
55	RESERVED	N/A	N/A	VDDLN	Not used in application, terminate with pull-down[b].
56	CPOL	Input	Digital	VDDLN	CPOL mode selection for SPI, read at power-up. Terminate with pull-up or pull-down[b].
57	MCLK	Input	Digital	VDDLN	Monitor clock input, terminate with pull-up[b].
58	N/C	N/A	N/A	N/A	Not used in application, no termination required
59	LPWM	Output	Digital	VDDLN	Laser power supply charging pulses
60	TLED_TRIG	Output	Digital	VDDLN	Test LED trigger
61	SYNC	Input/Output	Digital	VDDLN	Sync input/output
62	LTRIG	Output	Digital	VDDLN	Laser trigger
63	VDDLN	Supply	Power	VDDLN	Low-noise I/O supply, 3.3 V
64	RCLK	Input	Digital	VDDLN	Reference clock
65	VDDPLL	Supply	Power	VDDPLL	PLL supply, 2.5 V
66	VSS	Supply	GND	Common GND	Common GND
67	VDDIO	Supply	Power	VDDIO	Digital I/O supply, 3.3 V
68	MOSI_QO0	Input/Output	Digital	VDDIO	SPI input / QSPI output 0
69	MISO_QO1	Output	Digital	VDDIO	SPI output / QSPI output 1
70	QO2	Output	Digital	VDDIO	QSPI output 2
71	QO3	Output	Digital	VDDIO	QSPI output 3
72	SCK	Input	Digital	VDDIO	SPI clock
73	VSS EPAD	Supply	GND	Common GND	Common GND. EPAD for thermal heat sink. Soldering is required.

[b] For stable operation, external 10 kΩ ± 10% resistors are required.

4. IC Characteristics

4.1. Absolute Maximum Ratings

This section specifies the stress levels that, if exceeded, may cause permanent damage to the device. However, these are stress ratings only, and functional operation of the LCA2 LeddarCore at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Also, exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 – Absolute maximum ratings

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
Supply Voltage						
V_{DDC}, V_{DDA}, V_{DDA_REF}	Voltage at all pins of 1.2 V rail	To V_{SS}	–0.3		1.32	V
V_{DDPA_TIA}, V_{DDPA_BUF}, V_{DDPLL}	Voltage at all pins of 2.5 V rail	To V_{SS}	–0.3		2.75	V
V_{DDLN}, V_{DDIO}	Voltage at all pins of 3.3 V rail	To V_{SS}	–0.3		3.6	V
Input Pins						
I_{PD}	Maximum current into PD inputs[c]	PD inputs AC coupled	–1		2000	µA
V_{IO}	Maximum voltage applied to digital inputs	To V_{SS}, device supplied $V_{DDIO} \geq V_{DDIO\_min}$	–0.3		3.6	V
		To V_{SS} if V_{DDIO} not supplied	–0.3		0.5	V
V_{LN}	Maximum voltage applied to digital low-noise inputs	To V_{SS}, device supplied $V_{DDLN} \geq V_{DDLN\_min}$	–0.3		3.6	V
		To V_{SS} if V_{DDLN} not supplied	–0.3		0.5	V
V_{MNT}	Maximum voltage applied to analog monitoring inputs LPS_MNT and PDPS_MNT	To V_{SS}, device supplied $V_{DDPA} \geq V_{DDPA\_min}$	–0.3		2.75	V
		To V_{SS} if V_{DDPA} not supplied	–0.3		0.5	V
Thermal Ratings						
T_A	Operating ambient temperature[d]	According to JESD51-2	–40		105	°C
T_J	Operating junction temperature		–40		125	°C
T_{STG}	Storage temperature		–50		150	°C
ESD Protection						
V_{HBM}	ESD – Human body model (HBM)		–2000		2000	V
V_{CDM}	ESD – Charged device model (CDM): corner pins		–750		750	V
	ESD – Charged device model (CDM): all other pins		–500		500	V

[c] Negative current generated by transient response of external AC coupling capacitor C_{PD_AC} tolerated without device degradation.

[d] Operating life exposure qualified for 2100 hours at 105°C ambient.

4.2. Recommended Operating Conditions

Table 3 – Recommended operating conditions, general LCA2 LeddarCore IC

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
LCA2 Supply Voltage						
V_{DDC}	Operation voltage, digital core		1.14	1.2	1.26	V
V_{DDA}	Operation voltage, analog ADC		1.14	1.2	1.26	V
V_{DDA_REF}	Operation voltage, analog reference		1.14	1.2	1.26	V
V_{DDPA_TIA}	Operation voltage, analog front-end (refer to [e] to connect externally.)		2.375	2.5	2.625	V
V_{DDPA_BUF}	Operation voltage, analog front-end (refer to [e] to connect externally.)		2.375	2.5	2.625	V
V_{DDPLL}	Operation voltage, low-noise PLL		2.375	2.5	2.625	V
V_{DDLN}	Operation voltage, low-noise back-end (refer to [f] to connect externally.)		3.135	3.3	3.465	V
V_{DDIO}	Operation voltage, digital back-end (refer to [f] to connect externally.)		3.135	3.3	3.465	V
LCA2 Supply Noise						
$V_{n,VDDC}$ $V_{n,VDDIO}$	Supply voltage noise, digital core and back-end	BW = 10 Hz to 100 MHz			100	μV_{RMS}
$V_{n,VDDA}$ $V_{n,VDDA\_REF}$ $V_{n,VDDPA\_TIA}$ $V_{n,VDDPA\_BUF}$ $V_{n,VDPLL}$ $V_{n,VDDLN}$	Supply voltage noise, analog and low-noise rails	BW = 10 Hz to 100 MHz			50	μV_{RMS}

e V_{DDPA_TIA} and V_{DDPA_BUF} pins can be connected to the same power supply using an external filter.

f V_{DDIO} and V_{DDLN} pins can be connected to the same power supply using an external filter.

Table 4 – Recommended operating conditions, analog front-end

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
Analog Front-End, External Components						
I_{PD}	Photodiode signal current	Via external AC coupling	–1		200	µA
C_t	Photodiode terminal capacitance	Photodiode and PCB trace	1.5	3.2	10	pF
R_B	Photodiode biasing resistor			10		kΩ
C_{ac}	Photodiode AC coupling capacitor	In series to PD input		10		nF
t_{PD}	PIN photodiode pulse width, PD1 to PD32	Gaussian pulse measured at 50% of peak value		16		ns

Table 5 – Recommended operating conditions, digital interface (RCLK, MCLK)

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
f_{RCLK}	RCLK input frequency[g]	Tolerance ±100 ppm		25		MHz
DI_{RCLK}	RCLK input duty cycle		45	50	55	%
T_R, T_F	RCLK rise/fall time	20% to 80%		1	3	ns
J_{PER}	RCLK RMS period jitter	1.28 µs time window			6.6	ps
F_{MCLK}	MCLK input frequency for clock monitor[g]			4		kHz

4.3. Electrical and Thermal Characteristics

The electrical characteristics are valid within the following conditions:

- Parameters are tested in volume production (unless otherwise noted) over operating temperature range (unless otherwise noted) with operating conditions described in section 4.2.
- Photodiode input stimulation is done with a Gaussian pulse with a duration of 16 ns at 50% level.
- C_t = 3.2 pF
- SPI communication is halted during acquisition.

Table 6 – Electrical characteristics

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
Supply and Reference Current Consumption						
I_{DDC}	Current consumption, digital core (summary into all pins)	Static test[h]	11		62	mA
		LTRIG repetition rate = 51.2 kHz[i]		20	61.2[j]	mA
		LTRIG repetition rate = 102.4 kHz[i]		25	70.3[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		45	110.3[j]	mA
I_{DDA} I_{DDA_REF}	Current consumption, analog ADC and ADC reference (summary into	Static test[h]	465		700	mA
		LTRIG repetition rate = 51.2 kHz[i]		80	117.8[j]	mA

g Accuracy of clock monitoring is in linear relation to the accuracy of the externally provided MCLK. Further details are provided in the LCA2 Functional Safety Manual.

h Production test. Static measurement without continuous acquisition.

i Not tested in mass production. Parameter is guaranteed by design and/or characterization.

j 3-sigma value over process and temperature variation.

	all pins)	LTRIG repetition rate = 102.4 kHz[i]		170	213.4[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		570	661.5[j]	mA
I_{DDPA_TIA} I_{DDPA_BUF}	Current consumption, analog front-end (summary into all pins)	Static test[h]	145		560	mA
		LTRIG repetition rate = 51.2 kHz[i]		110	240.6[j]	mA
		LTRIG repetition rate = 102.4 kHz[i]		150	286.9[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		280	508[j]	mA
I_{DDPLL}	Current consumption, low-noise PLL	Static test[h]	10		15	mA
		LTRIG repetition rate = 51.2 kHz[i]		11	12.5[j]	mA
		LTRIG repetition rate = 102.4 kHz[i]		11	12.5[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		11	12.5[j]	mA
I_{DDLN}	Current consumption, low-noise back-end	Static test[h]	0.08		0.21	mA
		LTRIG repetition rate = 51.2 kHz[i]		8	15[j]	mA
		LTRIG repetition rate = 102.4 kHz[i]		8.5	18.5[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		9	20.5[j]	mA
I_{DDIO}	Current consumption, digital back-end	Static test[h]	0.13		0.25	mA
		LTRIG repetition rate = 51.2 kHz[i]		1.5	5[j]	mA
		LTRIG repetition rate = 102.4 kHz[i]		1.5	5[j]	mA
		LTRIG repetition rate = 409.6 kHz[i]		1.5	5[j]	mA
Operational Power Characteristics						
$P_{Operation}$	Total power consumption: power saving mode deactivated[i]	LTRIG repetition rate = 409.6 kHz			2242[j]	mW
	Total power consumption: power saving mode activated[i]	LTRIG repetition rate = 102.4 kHz			1121[j]	mW
		LTRIG repetition rate = 51.2 kHz			878[j]	mW
Package Thermal Characteristics						
Θ_{JC}	Thermal resistance, junction to case EPAD			1		°C/W
Θ_{JA}	Thermal resistance, junction to ambient	According to JESD51-2 and JESD51-7		22		°C/W
Light Acquisition Unit						
TIA_{GAIN}	Small signal trans-impedance	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX}	96	128	160	kΩ
		GAIN = 2 x 32k TDL32k = $3F_{HEX}$ TBUF = 07_{HEX}	48	64	80	kΩ
		GAIN = 2 x 8k TDL8k = $3F_{HEX}$ TBUF = 07_{HEX}	12	16	20	kΩ

		GAIN = 2 x 2k TDL2k = $3F_{HEX}$ TBUF = 07_{HEX}	3	4	5	kΩ
TIA_{LINEAR}	TIA input linear current range[i] (deviation ≤10% from value calculated at 1 µA)	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX}			5.2	µA
		GAIN = 2 x 32k TDL32k = $3F_{HEX}$ TBUF = 07_{HEX}			10.4	µA
		GAIN = 2 x 8k TDL8k = $3F_{HEX}$ TBUF = 07_{HEX}			41.6	µA
		GAIN = 2 x 2k TDL2k = $3F_{HEX}$ TBUF = 07_{HEX}			166.4	µA
BW_{LAU}	TIA bandwidth[i] (see Figure 3.)	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX}	20	28		MHz
		GAIN = 2 x 32k TDL32k = $3F_{HEX}$ TBUF = 07_{HEX}	17	32		MHz
		GAIN = 2 x 8k TDL8k = $3F_{HEX}$ TBUF = 07_{HEX}	29	41		MHz
		GAIN = 2 x 2k TDL2k = $3F_{HEX}$ TBUF = 07_{HEX}	30	41		MHz
ORT	Overload recovery time[i]	I_{PD} ≤2 mA Pulse width = 40 ns GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX}		41	57	ns
		I_{PD} ≤2 mA Pulse width = 40 ns GAIN = 2 x 32k TDL32k = $3F_{HEX}$ TBUF = 07_{HEX}		27	46	ns
		I_{PD} ≤2 mA Pulse width = 40 ns GAIN = 2 x 8k TDL8k = $3F_{HEX}$ TBUF = 07_{HEX}		18	31	ns

		I_{PD} ≤2 mA Pulse width = 40 ns GAIN = 2 x 2k TDL2k = $3F_{HEX}$ TBUF = 07_{HEX}		13	17	ns
LAU_{NOISE}	LAU input-referred noise (calculated)[i]	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX} PD pin open Single acquisition	3.2	7	16.3	nArms
	LAU input-referred noise (characterized)[i]	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX} PD pin terminated With 3.2 pF and 10 kΩ Single acquisition		17	27	nArms
	LAU output-referred noise (TIA + ADC)[h]	GAIN = 2 x 64k TDL64k = $3F_{HEX}$ TBUF = 07_{HEX} PD pin open Single acquisition	2	3.5	6	LSB
X_{talk}	Channel crosstalk[i]	Linear input range	–36	–40		dB
R_{LAU_ADC}	ADC resolution, light acquisition unit	Full scale		12		Bits
BIST						
I_{BIST}	Diagnostic current pulse amplitude	DTPC = 00_{HEX} TBUF = 07_{HEX}	96 mV/ TIA_{GAIN_min}	156 mV/ TIA_{GAIN}	240 mV/ TIA_{GAIN_max}	µA
		DTPC = 02_{HEX} TBUF = 07_{HEX}	192 mV/ TIA_{GAIN_min}	312 mV/ TIA_{GAIN}	480 mV/ TIA_{GAIN_max}	µA
		DTPC = 04_{HEX} TBUF = 07_{HEX}	288 mV/ TIA_{GAIN_min}	468 mV/ TIA_{GAIN}	720 mV/ TIA_{GAIN_max}	µA
		DTPC = 06_{HEX} TBUF = 07_{HEX}	384 mV/ TIA_{GAIN_min}	624 mV/ TIA_{GAIN}	960 mV/ TIA_{GAIN_max}	µA
		DTPC = 08_{HEX} TBUF = 07_{HEX}	480 mV/ TIA_{GAIN_min}	780 mV/ TIA_{GAIN}	1200 mV/ TIA_{GAIN_max}	µA
		DTPC = $0A_{HEX}$ TBUF = 07_{HEX}	576 mV/ TIA_{GAIN_min}	936 mV/ TIA_{GAIN}	1440 mV/ TIA_{GAIN_max}	µA
		DTPC = $0C_{HEX}$ TBUF = 07_{HEX}	672 mV/ TIA_{GAIN_min}	1092 mV/ TIA_{GAIN}	1680 mV/ TIA_{GAIN_max}	µA
		DTPC = $0E_{HEX}$ TBUF = 07_{HEX}	768 mV/ TIA_{GAIN_min}	1248 mV/ TIA_{GAIN}	1920 mV/ TIA_{GAIN_max}	µA

Voltage and Temperature Monitor						
V_{MNT}	Input voltage monitoring range LPS_MNT pin and PDPS_MNT pin	External voltage divider required	0		2	V
R_{in_MNT}	Input resistance, analog input LPS_MNT and PDPS_MNT			1		MΩ
C_{in_MNT}	Input capacitance, analog input LPS_MNT and PDPS_MNT			1		pF
d_{MNT}	Measurement accuracy, analog input voltage monitoring LPS_MNT and PDPS_MNT	6-sigma over PVT	–10.6		10.6	%
d_{1V2}	Measurement accuracy, power supply voltage monitoring, VDDC domain	6-sigma over PVT	–12.0		12.0	%
	Measurement accuracy, power supply voltage monitoring, VDDA domain	6-sigma over PVT	–9.9		9.9	%
d_{2V5}	Measurement accuracy, power supply voltage monitoring, 2.5V domains	6-sigma over PVT	–15.3		15.3	%
d_{3V3}	Measurement accuracy, power supply voltage monitoring, 3.3V domains	6-sigma over PVT	–15.3		15.3	%
TS_{Range}	Die temperature measurement range		–40		125	°C
d_{TS}	Temperature measurement accuracy		–6.6		6.6	°C
R_{ADC}	ADC resolution, monitoring ADC			10		Bits
Timings (Power-On, Power-Off, Reset)						
t_{RISE}	Supply rail rising slope, power-on	10% to 90% of VCC	0.05		50	V/ms
t_{PON1}	Supply settle time for power rails within same voltage domain, power-on[i]		0			ms
t_{PON2}	Supply delay time for power rails of different voltage domains, power-on[i]		1			ms
$t_{Startup}$	Device start-up time[i]	Keep RSTN low until the device is ready to operate. All supplies must be settled and clocks stable before device start-up is executed.			0.1	ms
t_{FALL}	Supply rail falling slope, power-on	90% to 10% of VCC	0.05		50	V/ms
t_{POFF}	Supply rail discharge time, power-off[i]		0			ms
t_{RSTN}	RSTN input, minimum pulse width[i]		50			ns
t_{IRQN}	Interrupt reaction time[i]	C_{LOAD} ≤15 pF			1	ms

Digital I/Os (RCLK, SYNC, MCLK, LPWM, TLED_TRIG, LTRIG, CPOL, CPHA)						
V_{IL}	Input detection range for “low” signal		–0.3		0.8	V
V_{IH}	Input detection range for “high” signal		2		$V_{DDLN\ (max)}$	V
V_{OL}	Output drive strength, low	I_{LOAD} ≤12 mA	V_{SS}		0.4	V
V_{OH}	Output drive strength, high	I_{LOAD} ≤12 mA	2.4		V_{DDLN}	V
R_{PD}	Input resistance, internal pull-down at pins RCLK, CPOL, CPHA	To V_{SS} rail	20		80	kΩ
R_{PU}	Input resistance, internal pull-up at pin MCLK	To V_{DD} rail	20		80	kΩ
C_{SYNC}	Load capability, SYNC[i]				5	pF
C_{LTRIG}	Load capability, LTRIG[i]				15	pF
C_{TLED_TRIG}	Load capability, TLED_TRIG[i]				15	pF
C_{LPWM}	Load capability, LPWM[i]				15	pF
Digital I/Os (RSTN, IRQN, and SPI Interface)						
V_{IL}	Input detection range for “low” signal		–0.3		0.8	V
V_{IH}	Input detection range for “high” signal		2		$V_{DDIO\ (max)}$	V
V_{OL}	Output drive strength, low	I_{LOAD} ≤4 mA	V_{SS}		0.4	V
V_{OH}	Output drive strength, high	I_{LOAD} ≤4 mA	2.4		V_{DDIO}	V
R_{PD}	Input resistance, internal pull-down at pins MOSI_QO0, SCK	To V_{SS} rail	20		80	kΩ
R_{PU}	Input resistance, internal pull-up at pins RSTN, CSN	To V_{DD} rail	20		80	kΩ

5. Features and Description

5.1. Functional Description

The LCA2 LeddarCore architecture comprises a parallel multi-channel data acquisition system with an SPI interface for data exchange with an external microcontroller. This integrated mixed-signal system is capable to serve an array of 32 PIN photodiodes enabling time-of-flight and intensity measurements. The device can be configured according to use cases for analog parameters (e.g., TIA gain, bandwidth) as well as for digital functionality (e.g., number of data acquisitions, oversampling, accumulation, dithering).

Configuration and data acquisition are initiated through the SafeSPI interface by an external master. The data can be read out through standard SPI or quad SPI through the same interface pins.

5.2. Block Diagram

The functional block diagram is provided in Figure 2. The main functionality can be described as the generation of a trigger signal for an external infrared laser source, the analog-to-digital conversion of the received “light radiation energy”, and the storage of the digitized raw traces in memory provided to an external post-processing microprocessor. A frame scan is completely scheduled by the LCA2 LeddarCore core controller running autonomously and parallel in each light acquisition unit (LAU1 to LAU8).

5.3. Analog Front-End (PD1 to PD32, L_MNT)

The analog front-end consists of trans-impedance amplifier (TIA) inputs to receive the photodiode currents from 32 parallel current sources. Multiplexers are placed in front of the TIAs to select 16 input channels at a time. The multiplexer must be configured before a frame scan is applied and kept unchanged during the whole light acquisition phase.

Photodiode current is provided by an external 32-channel pin photo-array and fed through dedicated AC coupling capacitors to each of the PD inputs. The AC coupling is required to remove DC offset from ambient light. Key requirements for the analog front-end inputs are listed in Table 3.

The same requirements also apply to the laser monitor input (L_MNT), where an external photodiode can be connected to monitor the functionality and efficiency of an external laser diode.

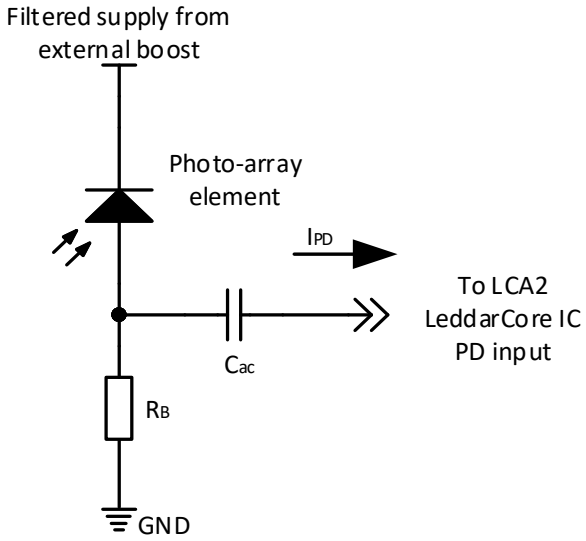

Figure 4 – Photodiode input configuration

5.4. Light Acquisition Unit (LAU1 to LAU8)

Each of the 8 light acquisition units (LAU 1 – 8) contains two TIAs with track-and-hold circuit and a 12-bit dual-channel ADC with dynamic power scaling capability. This allows an interlaced scan of 32 channels in total (16 odd and 16 even channels with two frame scans). The TIA can be configured with gain settings up to 128 k to allow a wide linear dynamic range.

5.5. LCA2 Core Controller

A frame scan of 16 even or odd channels contains minimum one triggered laser pulse and its reflection acquired autonomously. Flexible to a customer use case, an operation mode can be selected and executed by the programmable state machine. According to customer requirements, performance selectors can be combined within the following ranges:

- Sampling frequency is 100 MHz for 16 parallel channels.
- Each channel can sample up to 1024 consecutive ADC measurement points per laser pulse.
- Oversampling (up to 32 times) improves the time resolution of two adjacent ADC measurement points, which increases the LiDAR ranging accuracy.
- Accumulation of multiple laser pulses (up to 1024) allows to increase the signal-to-noise ratio and detect weak reflecting targets.
- Laser pulse repetition rate up to 409.6 kHz.
- Dithering time generator to avoid interferences with other LiDAR systems by adding randomness to the laser pulse repetition rate.

Operation modes can be combined, but limitations may apply due to internal memory depth and the required frame rate.

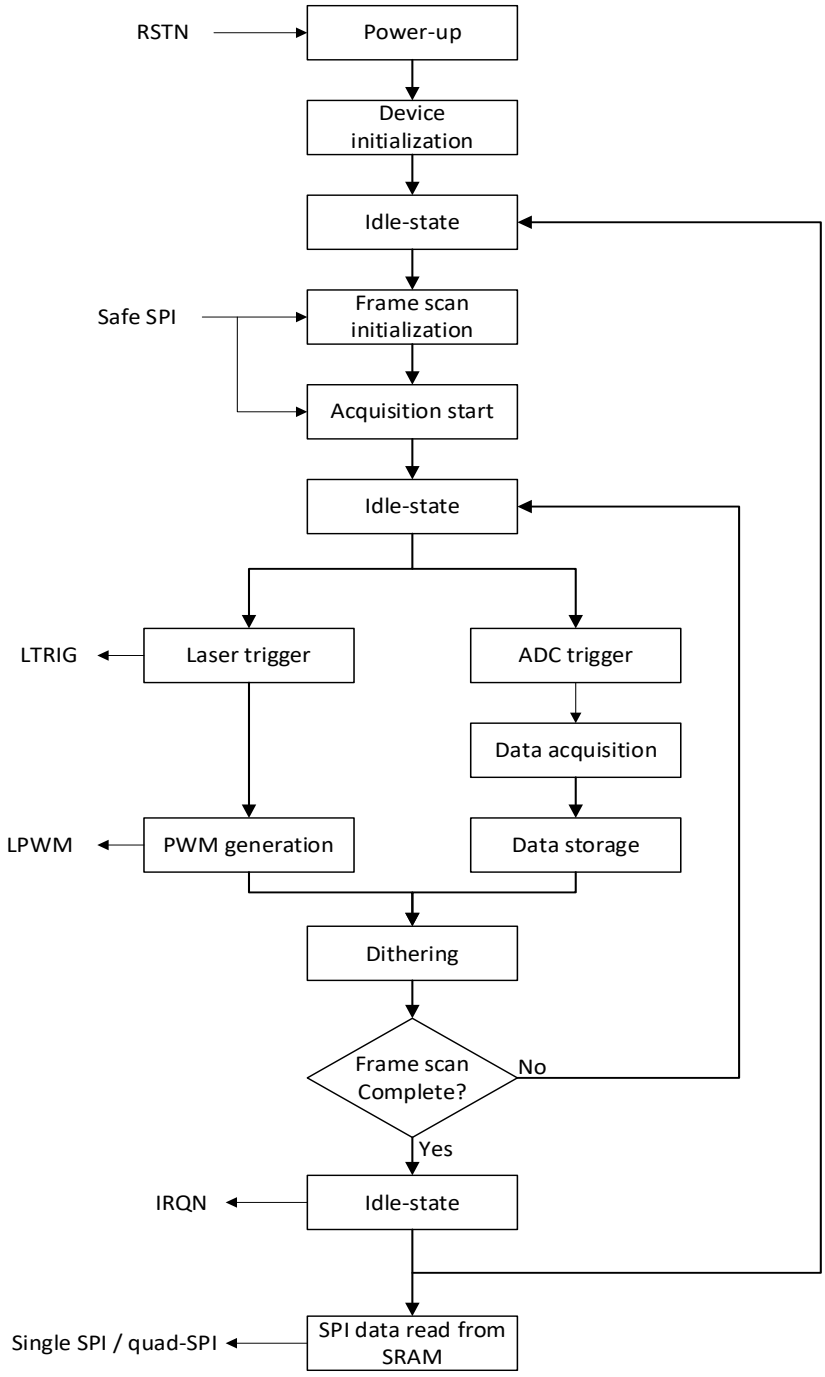

Figure 5 – General system and data acquisition state machine

5.6. Laser Pulse Generator (LTRIG, TLED_TRIG)

LTRIG signal enables the laser when the ToF (time-of-flight) ADC acquisition is started. TLED_TRIG enables a test LED which directly points to the photo-array for test purposes. Pulse width is programmable for both trigger signals. ADCs within the light acquisition units (LAU1 to LAU8) are triggered synchronous to the light sources, which is key to determine the object distance through ToF measurement. Oversampling and a programmable fine delay increases accuracy and allows to reduce influence of parasitic signal delays. Pseudo-random dithering decreases disturbances caused by other LiDAR systems nearby.

5.7. Primary/Secondary Operation Mode Using SYNC

In case of a primary/secondary operation (where two photo-arrays and two LCA2 LeddarCore ICs are combined to a single LiDAR system), the clock signal needs to be routed in a Y- or T-connection to both LCA2 LeddarCore ICs. The clock chip needs to be placed in the middle to have the same signal path length. Any difference in the propagation delay results in a distance error by the time-of-flight measurement. The RCLK signals of primary and secondary need to be phased synchronous. The SYNC pins of both LCA2 LeddarCore ICs must be connected together.

5.8. Laser Supply Control (LPWM) and Monitor (LPS_MNT)

LPWM digital output provides a programmable PWM sequence which controls an external boost regulator. This provides the power to the laser diode, discharged by the LTRIG laser pulse trigger. The PWM sequence allows to control the total energy pumped into a storage capacitor.

Energy discharge into a laser diode is initiated by the LTRIG signal. Voltage drop on the capacitor during the discharge can be measured with monitor input LPS_MNT to control and optimize the laser energy.

5.9. Functional Safety Monitoring Features

Several functional safety monitoring features allow in-operation feedback of system health and optimized operation conditions:

- **Device temperature:** Periodic monitoring of internal device temperature
- **Operation voltages:** Periodic monitoring of all IC power supplies
- **Operation of external components:**
  - Periodic monitoring of laser and photodiode power supplies
  - Laser monitoring photodiode and test LED for photodiode monitoring
- **BIST data path self-check:** A current pulse can be injected at the MUX input before the TIA to validate the complete acquisition and data path.
- **Data and protocol integrity:** CRC implemented in SafeSPI and with data transfers.

5.10. Interrupt and Reset (IRQN, RSTN)

IRQN is an open-drain output used to report errors to the host MCU.

RSTN is an input to allow the host MCU to execute a digital core reset during power-on and in case of an error.

5.11. Digital Interfaces (SafeSPI, Single SPI, and Quad SPI)

The LCA2 LeddarCore IC contains a SafeSPI slave for configuration and operation control. The SafeSPI protocol is implemented according to SafeSPI Specification V1.0 (June 3, 2016). For burst read of acquired frame scan data, the device supports standard single-bit SPI and quad SPI via the same SPI interface pins (pins 68 to 72). Therefore, three transaction-type commands are defined as described in Table 8.

Addressing the LCA2 LeddarCore IC with the chip select pin CSN allows operating two LCA2 LeddarCore ICs in primary/ secondary operation on the same bus.

5.11.1 Selectable CPOL and CPHA for SPI/QSPI Interface

All four mode configurations for CPOL and CPHA are supported. They are defined during power-up by resistors on the associated configuration pins.

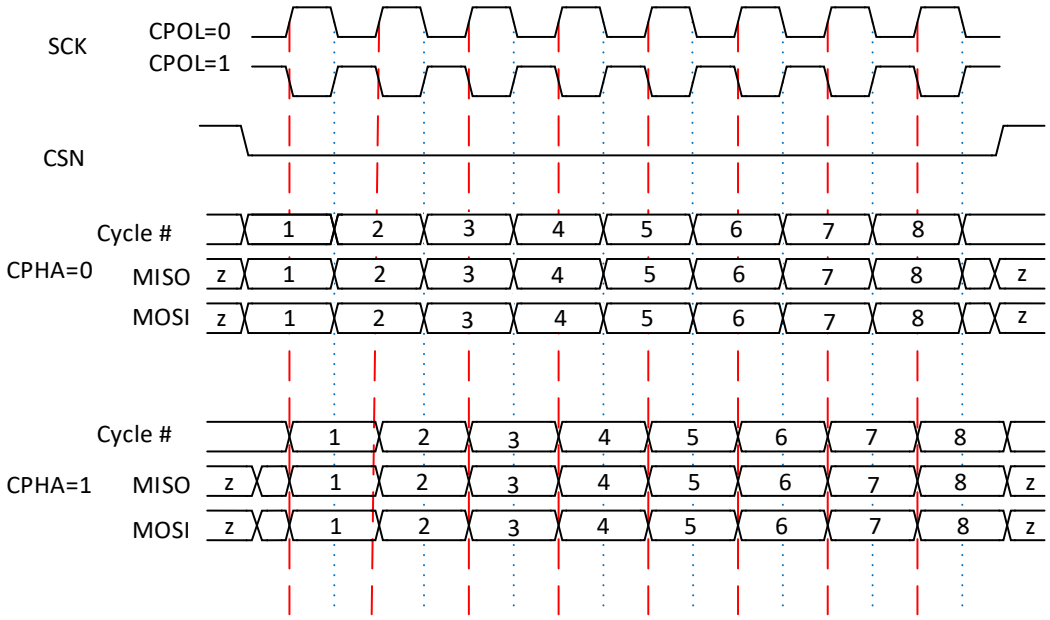

Figure 6 – SPI/QSPI interface timing diagram

LCA2 SPI/QSPI clock mode definitions

1. SPI/QSPI clock polarity selection:
   a. CPOL = 0 (pull-down) SPI clock is not inverted
   b. CPOL = 1 (pull-up) SPI clock is inverted
2. SPI/QSPI clock phase selection:
   a. CPHA = 0 (pull-down) "data capture" @ SCK leading clock edge (red/dashed lines)
      "data shift" @ SCK trailing clock edge (blue/dotted lines)
   b. CPHA = 1 (pull-up) "data capture" @ SCK trailing clock edge (blue/dotted lines)
      "data shift" @ SCK leading clock edge (red/dashed lines)

The SPI/QSPI slave operates in all modes selectable by CPOL ("clock polarity" selection) and CPHA ("clock phase" selection).

5.11.2 SPI Timing

Figure 7 shows a single-SPI mode bit ordering diagram corresponding to the mode where CPOL = 0 and CPHA = 1. All data is transferred with the MSB first. Timing data for LCA2 LeddarCore's 50 MHz interface operation is included below in Figure 8 to Figure 10 and Table 7.

CPOL=0 and CPHA =1

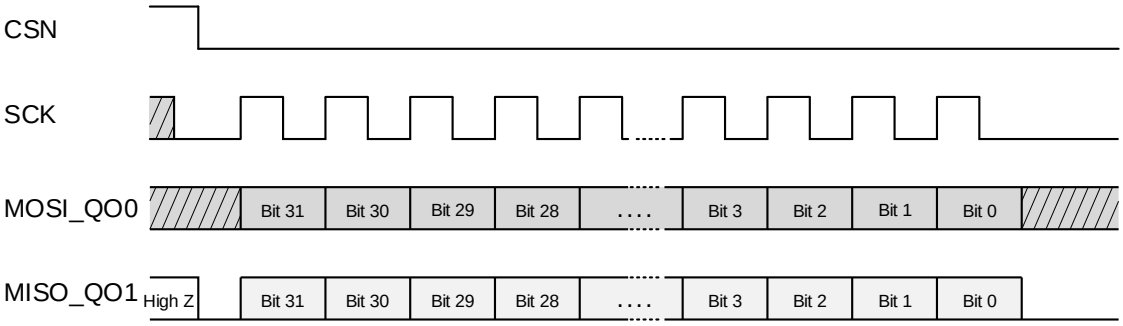

Figure 7 – Single-SPI bit ordering diagram

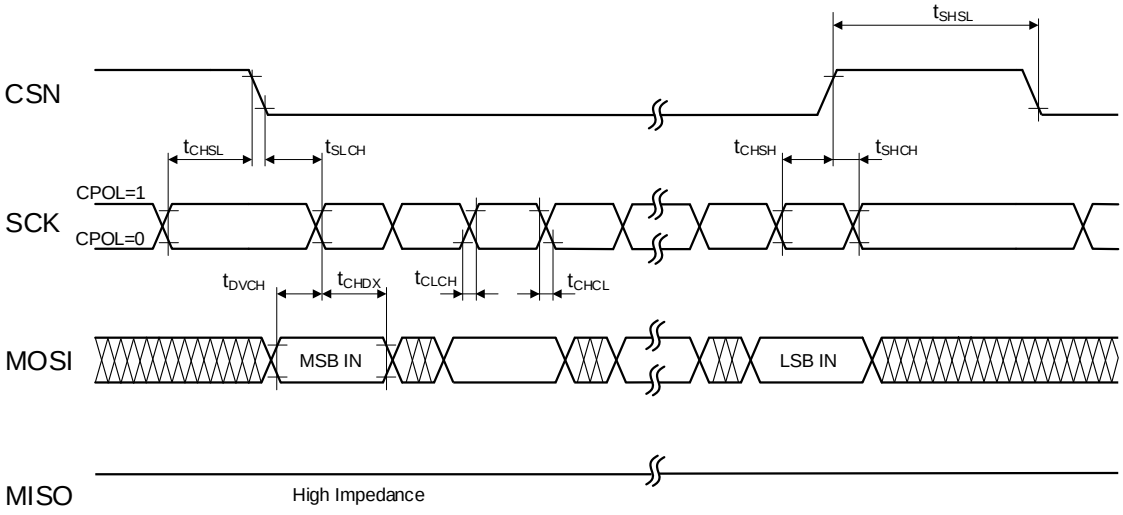

Figure 8 – SPI input timing diagram

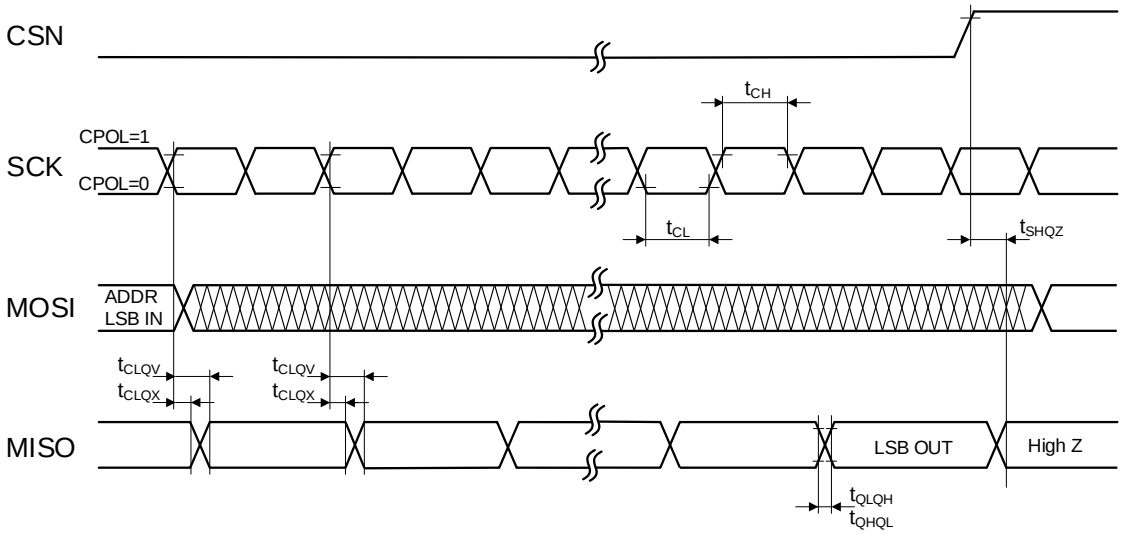

Figure 9 – SPI output timing diagram

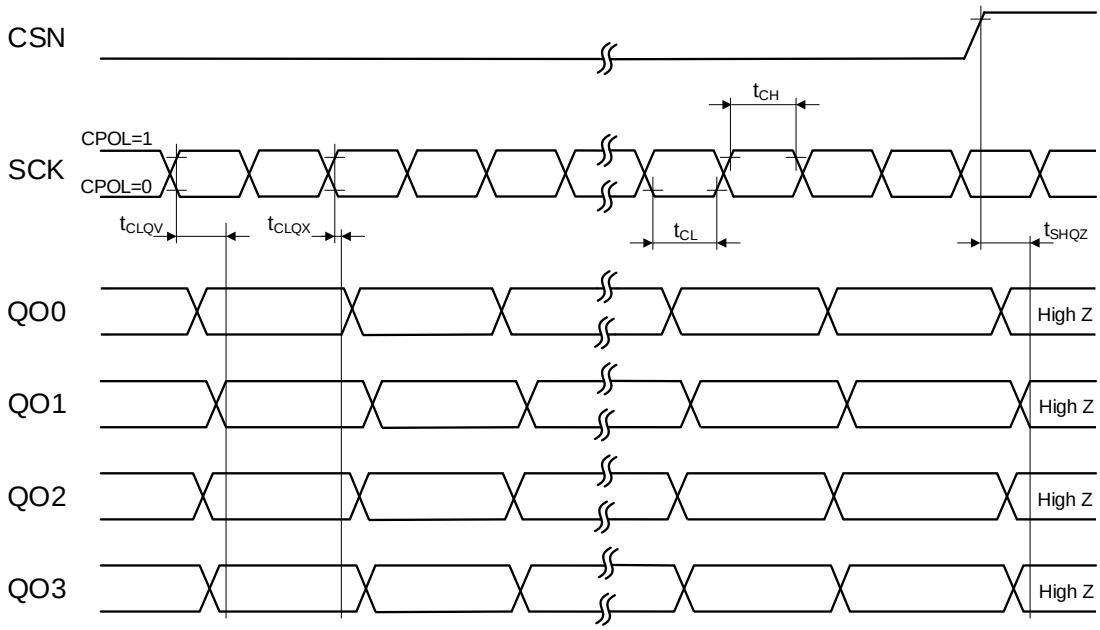

Figure 10 – Quad-SPI output timing diagram

Table 7 – SPI timing

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
f_{SCK}	SPI clock frequency, single SPI (write)	C_{LOAD} ≤15 pF Drive strength = 4 mA	1		50	MHz
	SPI clock frequency, single SPI (read)	C_{LOAD} ≤15 pF Drive strength = 4 mA	1		50	MHz
	SPI clock frequency, quad SPI (read)	C_{LOAD} ≤15 pF Drive strength = 4 mA	1		50	MHz
t_{CHSL}	SCK to CSN inactive hold time[k]		10			ns
t_{SLCH}	CSN active to SCK setup time[k]		30			ns
t_{CLCH}	SCK rise time[k]		0		2	ns
t_{CHCL}	SCK fall time[k]		0		2	ns
t_{CH}	SCK high time[k]		8			ns
t_{CL}	SCK low time[k]		8			ns
t_{CHSH}	CSN active hold time[k]		10			ns
t_{SHCH}	CSN inactive setup time[k]		10			ns
t_{SHSL}	CSN deselect time[k]		100			ns
t_{DLDH}	Data in rise time[k]		0		2	ns
t_{DHDL}	Data in fall time[k]		0		2	ns
t_{DVCH}	Data in setup time[k]		2			ns
t_{CHDX}	Data in hold time[k]		4			ns
t_{CSQV}	CSN low to data output valid[k]				20	ns

[k] Not tested in mass production. Parameter is guaranteed by design and/or characterization.

t_{CLQV}	SCK shift to data output valid (single SPI)[k]				8	ns
	SCK shift to data output valid (quad SPI)[k]				8	ns
t_{CLQX}	Data out hold time[k]		0			ns
t_{QLQH}	Data out rise time, drive strength = 4 mA[k]	C_{LOAD} ≤15 pF	0.3		2	ns
t_{QHQL}	Data out fall time, drive strength = 4 mA[k]	C_{LOAD} ≤15 pF	0.3		2	ns
t_{SHQZ}	CSN to data out disable time[k]		1		20	ns
$T_{WR\_to\_RD}$	SPI bus turnaround time, SafeSPI write to quad-SPI read[k]		$8 * 1/f_{SCK}$			

5.11.3 SafeSPI Mode Protocol Structure

SafeSPI data exchange is based on the transmission of 16-bit words inside a 32-bit SafeSPI protocol frame as shown in Figure 11. To initiate a transfer, the master asserts the CSN signal and send 10-bit TA (must be zero), 3-bit reserved (must be zero), a 4-bit command, and a 12-bit option followed by a 3-bit CRC checksum. The slave shifts out the internal IC status simultaneously with one frame delay. In the case of a write transfer, the master continues to shift out 32-bit words via the MOSI line. The slave sets all bits of the read data to "0". In the case of a read transfer, the slave shifts out the data to be read via the MISO line and ignores the write data. For further details, see SafeSPI Specification V1.0 at www.safespi.org/.

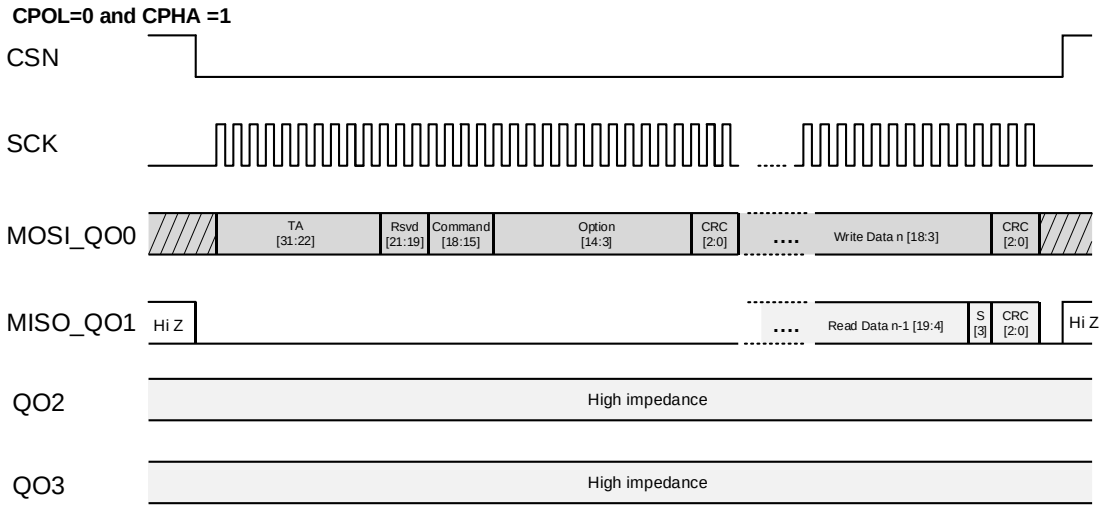

Figure 11 – SafeSPI protocol frame

Table 8 – SPI mode select and addressing

Command (4-Bit)	Option (12-Bit)	Protocol
1_{HEX}	Register address	Write register through SafeSPI
2_{HEX}	Register address	Read register through SafeSPI
3_{HEX}	Bit 0 = "0": Buffer A Bit 0 = "1": Buffer B Bit 1 = "0": Single SPI Bit 1 = "1": Quad SPI	Read measurement data memory via single SPI or quad SPI

Table 9 – SafeSPI protocol (read), MOSI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame 1	TA (must be 0_{BIN})										Reserved (0_{BIN})			Command				Option (register address)											CRC			
Frame 2 - n	TA (must be 0_{BIN})										Reserved (0_{BIN})			Dummy data (0_{BIN})																CRC			

Table 10 – SafeSPI protocol (read), MISO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame 1	D	SA										S1	Data (0_{BIN})																SO	CRC		
Frame 2 - n	D	SA										S1	Data																SO	CRC		

Table 11 – SafeSPI protocol (write), MOSI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame 1	TA (must be 0_{BIN})										Reserved (0_{BIN})			Command				Option (register address)											CRC			
Frame 2 - n	TA (must be 0_{BIN})										Reserved (0_{BIN})			Write data																CRC			

Table 12 – SafeSPI protocol (write), MISO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame 1	D	SA										S1	Data (0_{BIN})																SO	CRC		
Frame 2 - n	D	SA										S1	Dummy data																SO	CRC		

5.11.4 Standard SPI Mode Protocol Structure

Standard SPI data exchange is used for reading out the memory. It can be executed in single SPI or quad SPI mode, which allows higher data rate. The data readout has to be initiated with a SafeSPI write command. In single SPI mode, the data shows up on MISO_QO1 pin immediately (see Figure 12). In quad SPI mode, an SPI bus turnaround time of 8 dummy clocks is required before data are provided to QO0, QO1, QO2, and QO3 (see Figure 13).

CPOL=0 and CPHA =1

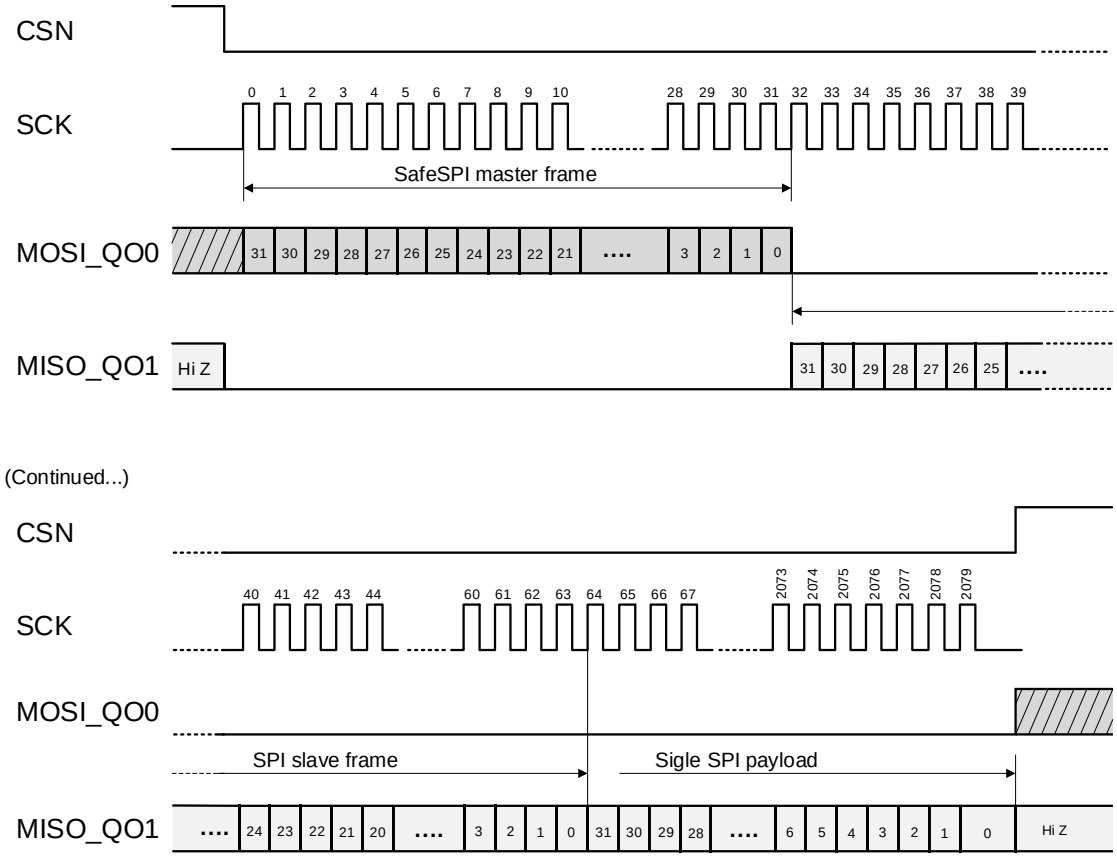

Figure 12 – Standard SPI scan data read protocol (single SPI)

CPOL=0 and CPHA =1

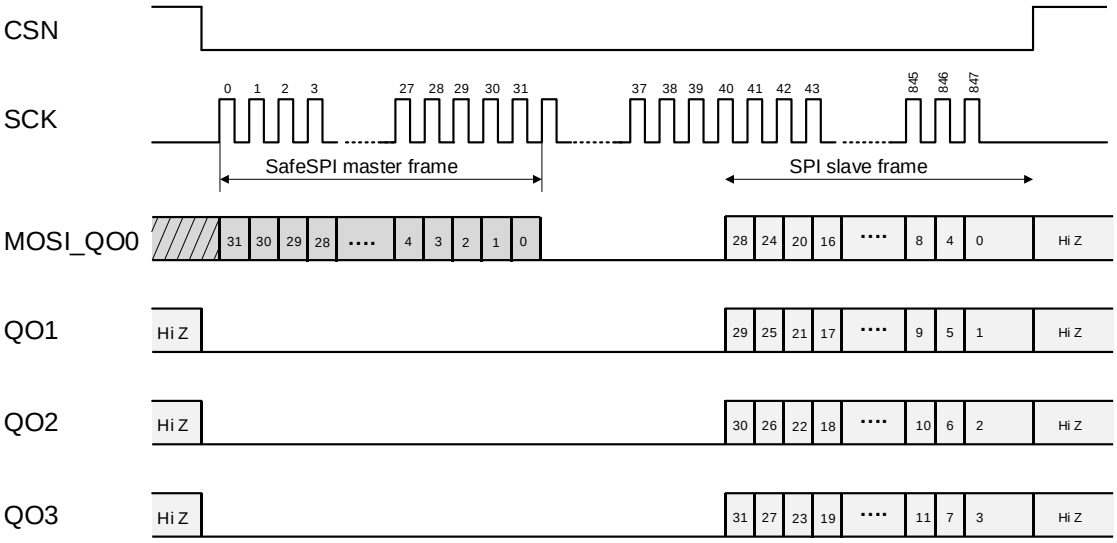

Figure 13 – Standard SPI scan data read protocol (quad SPI)

6. Package Drawings

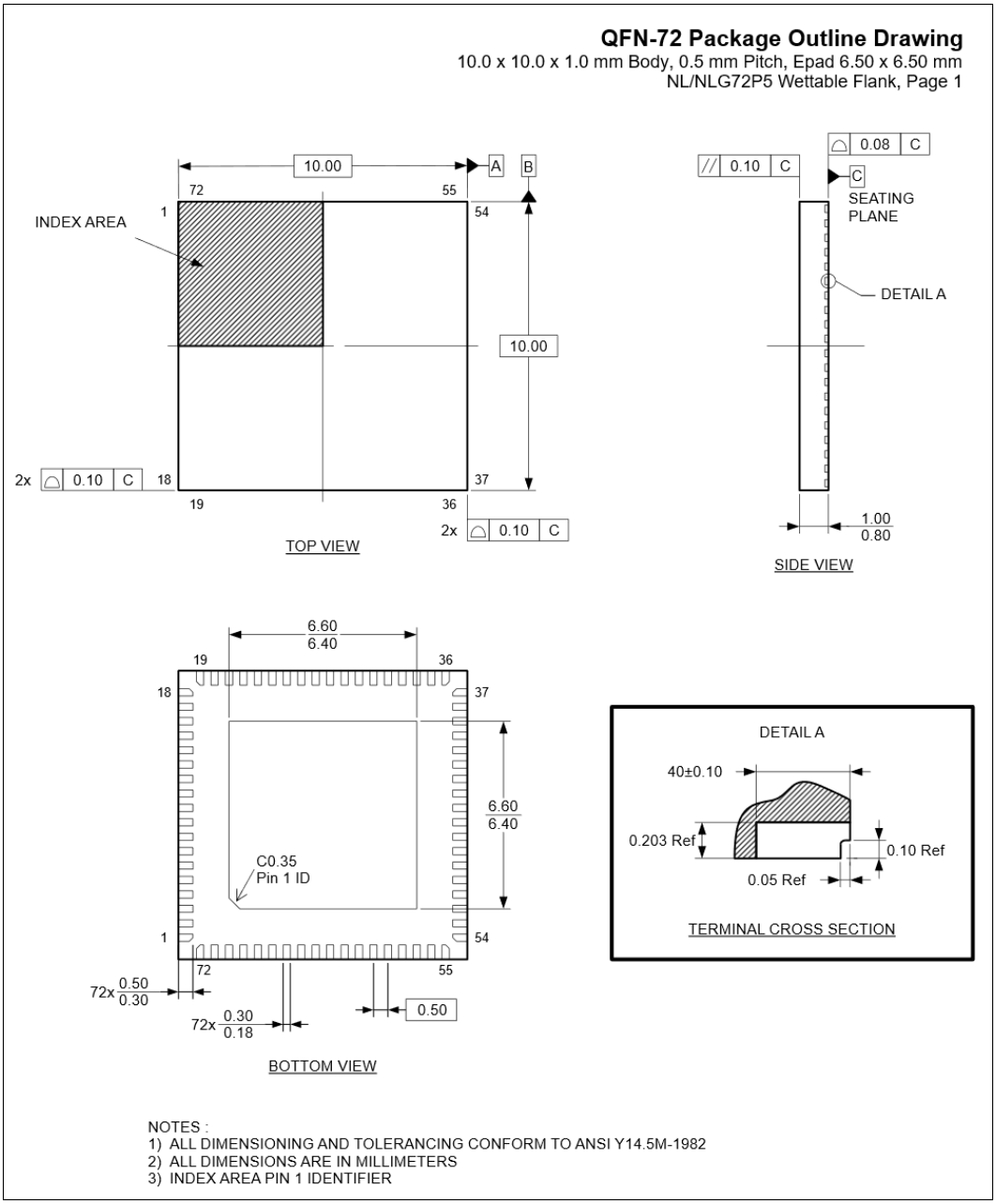

Figure 14 – Package outline drawing

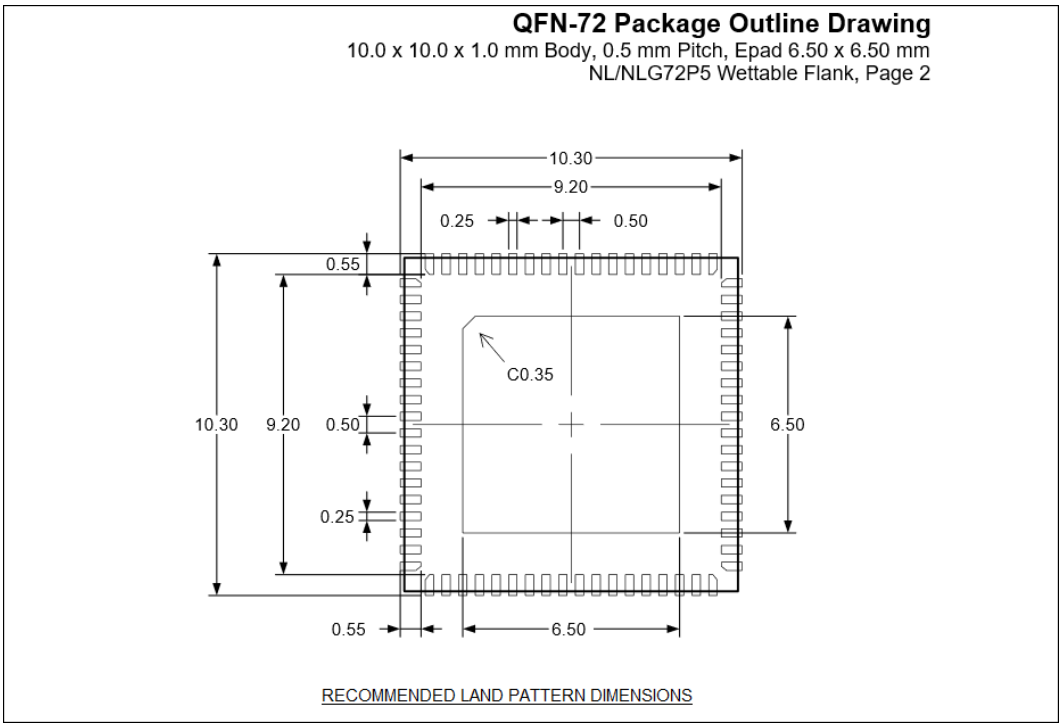

Figure 15 – Recommended land pattern

7. Package Markings

Line 1 shows the company logo (LeddarTech®).

Line 2 shows the part number (LCA200B1-2), where:

LCA200B1 =	Product family and sub-product number
00 =	Variant
B1 =	Revision
2 =	Temperature grade

Line 3 shows the manufacturing information (#YYWW$)

# =	Device stepping
YY =	Last digits of manufacturing year
WW =	Week the part was assembled
$ =	Assembly site code

Characters next to pin 1 marking:

Lot =	Lot number
COO =	Country of origin

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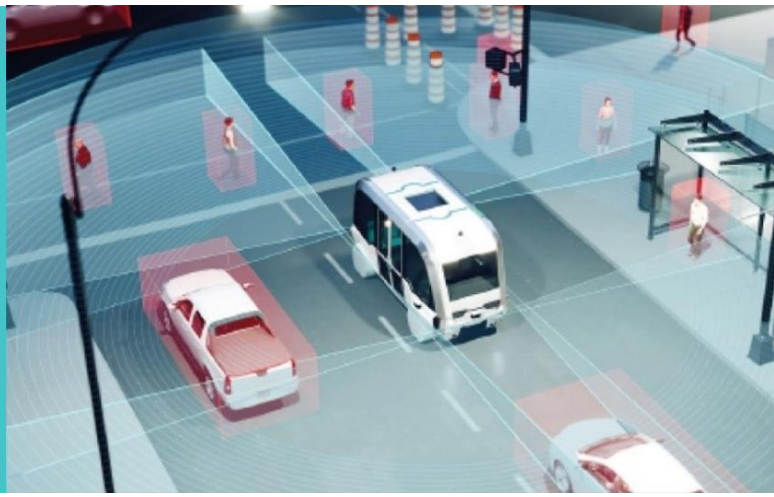
LeddarTech is a leader in environmental sensing platforms for autonomous vehicles and advanced driver assistance systems. Founded in 2007, LeddarTech has evolved to become a comprehensive end-to-end environmental sensing company by enabling customers to solve critical sensing and perception challenges across the entire value chain of the automotive and mobility market segments. With its LeddarVision™ sensor-fusion and perception platform and its cost-effective, scalable, and versatile LiDAR development solution for automotive-grade solid-state LiDARs based on the LeddarEngine™, LeddarTech enables Tier 1-2 automotive system integrators to develop full-stack sensing solutions for autonomy level 1 to 5. These solutions are actively deployed in autonomous shuttles, trucks, buses, delivery vehicles, smart cities/factories, and robotaxi applications. The company is responsible for several innovations in cutting-edge automotive and mobility remote-sensing applications, with over 95 patented technologies (granted or pending) enhancing ADAS and autonomous driving capabilities.

For more information: sales@leddartech.com



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