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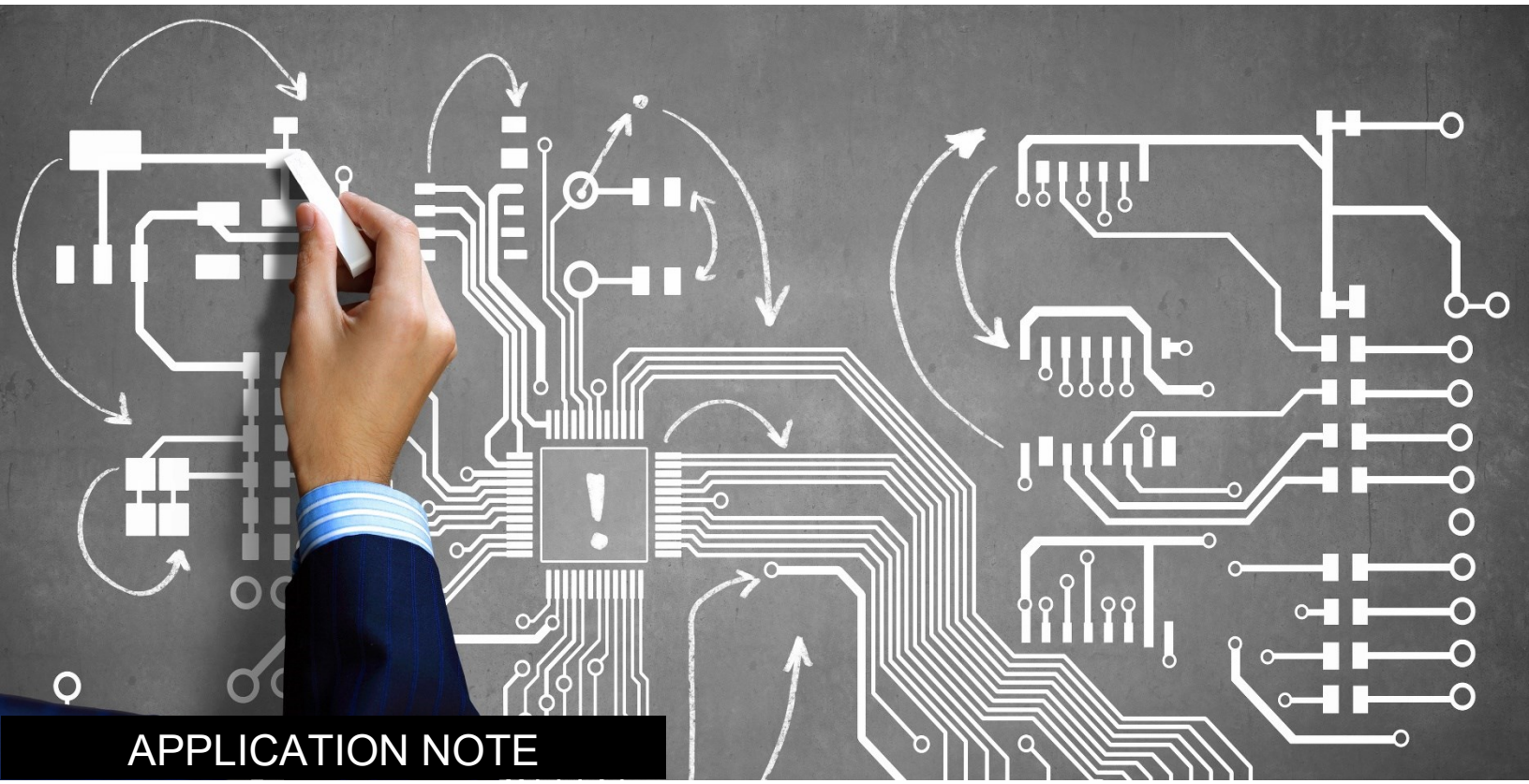
Solving Critical Sensing, Fusion and Perception Challenges

DEVELOPER GUIDE

LCA2 LeddarCore Power Supply Design and Sequencing



Abstract

The LCA2 LeddarCore™ requires several different supply rails. The power rails are divided between the digital and analog domains. Some of these supplies have rather specific noise and filtering requirements. The LCA2 LeddarCore™ SoC also requires these power supplies to be sequenced in a defined order to ensure the correct operation of the chip and to prevent damage or accelerated wear. This Developer Guide, meant for the developers of LCA2 LeddarCore SoC-based LiDARs, outlines the details of a successful power supply implementation and associated recommendations.

LCA2 LeddarCore Power Requirements

Power Rails

The LCA2 LeddarCore requires eight different external power rails to function. They consist of the following:

1. **VDDA (1.2 V)** – ADC-Cores
2. **VDDA_REF (1.2 V)** – ADC-Reference – Low-noise
3. **VDDC (1.2 V)** – ADC-Logic, Monitor-Logic, Core-Logic and RAM
4. **VDDIO (3.3 V)** – Digital I/O
5. **VDDLN (3.3 V)** – Low-noise I/O
6. **VDDPA_BUF (2.5 V)** – Analog front end
7. **VDDPA_TIA (2.5 V)** – Trans-impedance amplifiers
8. **VDDPLL (2.5 V)** – Phase-locked loop

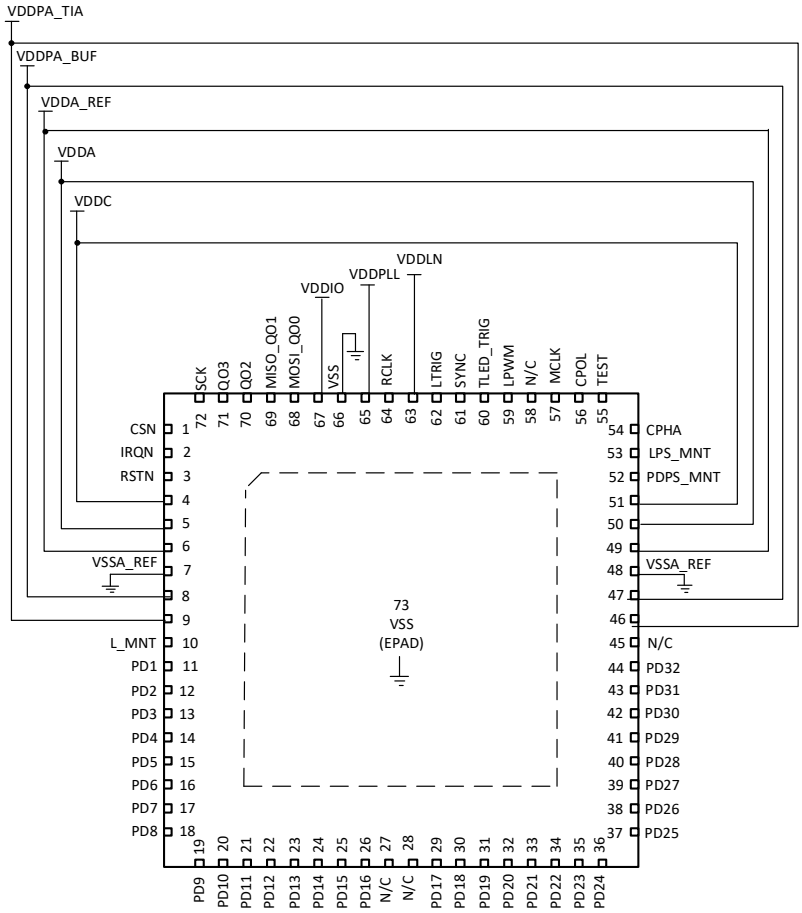


Figure 1 – Pinout with connections to supply rails

Power Rail Requirements

Some of the supply rails used in the LCA2 have strict noise requirements due to their use in the sensitive analog signal path. The current and noise requirements are summarized in Table 1 below.

Table 1 – LCA2 LeddarCore power supplies

Supply Domain	Supply Voltage (V)	Used in LCA2 LeddarCore for	Max DC Current[1] (mA)	LDO Noise Requirement (10 Hz – 100 MHz)	LDO PSRR Requirement	C_{out} at Dedicated LDO Output[2]	C_{in} at LCA2 LeddarCore Supply Pins[3]
VDDA, VDDA_REF	1.2	ADC-Core, ADC Reference	661.5	≤50 μV_{RMS}	≥60 dB	≥10 µF	470 pF and 100 nF
VDDC	1.2	ADC-Logic, Monitor-Logic, Core-Logic, and RAM	110.3	≤100 μV_{RMS}	≥40 dB	≥3.3 µF	470 pF and 100 nF
VDDIO	3.3	Digital I/O, QSPI, IRQN, RSTN	65	≤100 μV_{RMS}	--	≥2.2 µF	470 pF and 100 nF
VDDLN	3.3	Low-Noise I/O, LTRIG, LPWM, TLED_TRIG, SYNC, JTAG	20.5	≤50 μV_{RMS}	≥60 dB	≥2.2 µF	470 pF and 100 nF
VDDPA_BUF, VDDPA_TIA	2.5	ADC-FrontEnd, Monitor-FrontEnd, TIA, Bias, Bandgap	508	≤50 μV_{RMS}	≥60 dB	≥3.3 µF	470 pF and 100 nF
VDDPLL	2.5	PLL[4]	12.5	≤50 μV_{RMS}	≥60 dB	--	470 pF and 100 nF
VDDPD[5]	1.2	L_MNT, PD1-PD32	--[5]	--	--	--	--

Power Domains

The LCA2 has three power domains for external I/O. These are VDDIO, VDDLN and VDDPD. It is important to consider them when interfacing to external components. In particular, the complete path from power supply to ground (return path) must be considered to prevent signal propagation and EMI/EMC issues.

1 Current consumption of LCA2 LeddarCore SoC with maximum performance. For Primary/Secondary mode operation using two LCA2 LeddarCore SoCs, the current consumption of the system will be doubled.

2 Make sure the minimum stability requirements for the selected LDO are met. Use X7R capacitors with stable temperature behavior, low ESR and proper voltage rating.

3 Both capacitors need to be placed as close as possible to each LCA2 LeddarCore SoC supply pin, with the 470 pF capacitor closer to the device pin and 100 nF right next to it. All capacitors should be X7R or better.

4 The external oscillator providing RCLK to the PLL should have similar low-noise requirements.

5 VDDPD is a power domain generated inside the chip. There are no external power pins, although it is derived from VDDPA_TIA.

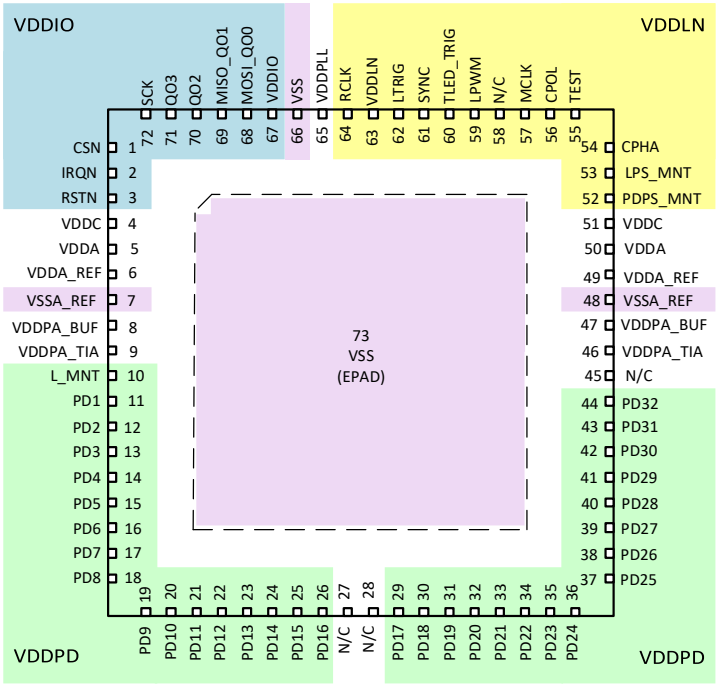


Figure 2 – LCA2 power domains

Ground

Like with any mixed-signal design, the importance of a good grounding scheme is significant. Since the LCA2 includes an analog-to-digital converter, it should be treated as one when doing the PCB design and layout. The recommended approach is to use a single-ground plane and segregate the sensitive analog return currents from the high-speed digital currents by careful component placement and partitioning the layout. If this is not possible, then the grounds can be separated into analog and digital grounds and be connected under the LCA2 package (at the VSS thermal pad). Separating the grounds also has many challenges, as the PCB designer must be careful not to lay any traces across the boundaries between grounds, keeping in mind that the return current for a given trace tends to circulate directly underneath the trace (the path of least inductance). In the specific context of a pulsed LiDAR, the laser driver will typically be the most power-hungry part of the circuit with high dI/dt (the rate of change of the current). The designer must ensure that the laser driver supply and ground have the smallest possible loop area and that the signals are routed away from the sensitive analog part of the circuit, as close as possible to the power supply.

There are many existing publications that cover analog/digital mixed signal design and PCB layout. Below are a few useful references to consider on the subject:

Ott, Henry W., Partitioning and Layout of a Mixed Signal PCB, Printed Circuit Design, June 2001.

Zumbahlen, Hank, Staying Well Grounded, Analog Dialogue 46-06, June 2012.

Power-On/Off Rail Sequencing

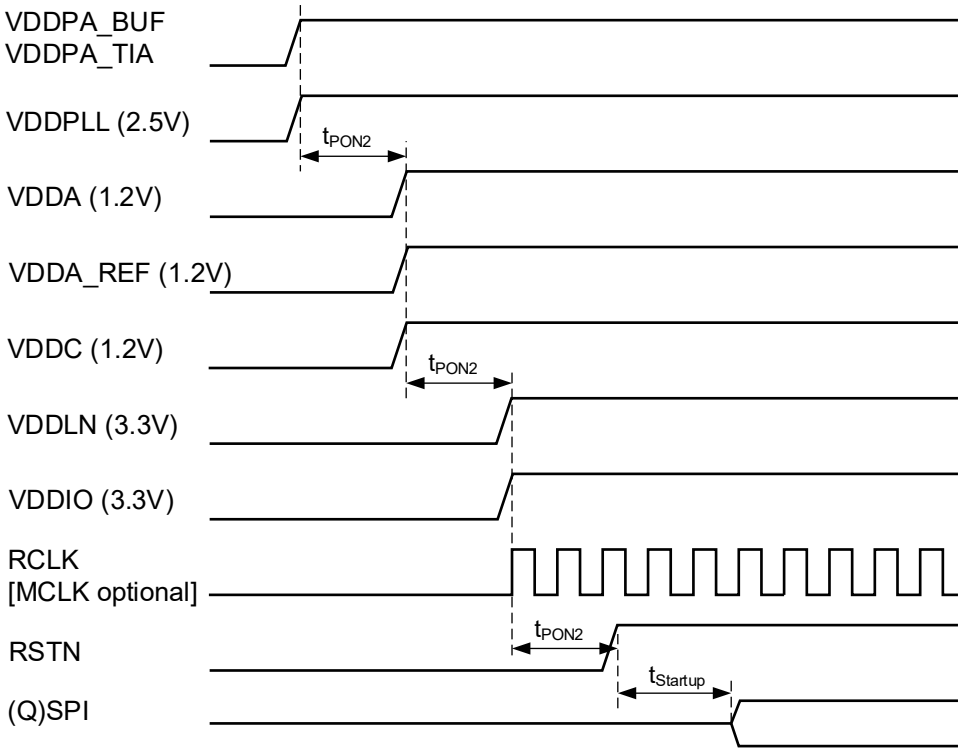


Figure 3 – Power-on sequencing

Like with many SoCs, the LCA2 has requirements as to what order the power rails have to come up and come down. Specifically, there are six events for the power-up sequence:

1. 2.5 V rails: VDDPA_TIA, VDDPA_BUF, VDDPLL
2. 1.2 V rails: VDDA, VDDA_REF, VDDC
3. 3.3 V rails: VDDLN, VDDIO
4. Enable the oscillator
5. Release reset signal
6. Start communication with the LCA2

The timing of these events is summarized in Table 2.

Table 2 – LCA2 power-on sequence timings

Symbol	Description	Min.	Max.	Unit
t_{PON2}	Time between enabling of the different voltage rails	1	--	ms
$t_{Startup}$	Time to boot after reset is released	0.1	--	ms

For power-down, it is required to apply the power-up sequence in reverse order:

1. Stop communication with the LCA2
2. Apply reset signal
3. Disable the oscillator
4. Remove the 3.3 V rails: VDDLN, VDDIO
5. Remove the 1.2 V rails: VDDA, VDDA_REF, VDDC
6. Remove the 2.5 V rails: VDDPA_TIA, VDDPA_BUF, VDDPLL

There is no constraint on required timing as long as this sequence is followed.

Power Supply Design and Implementation

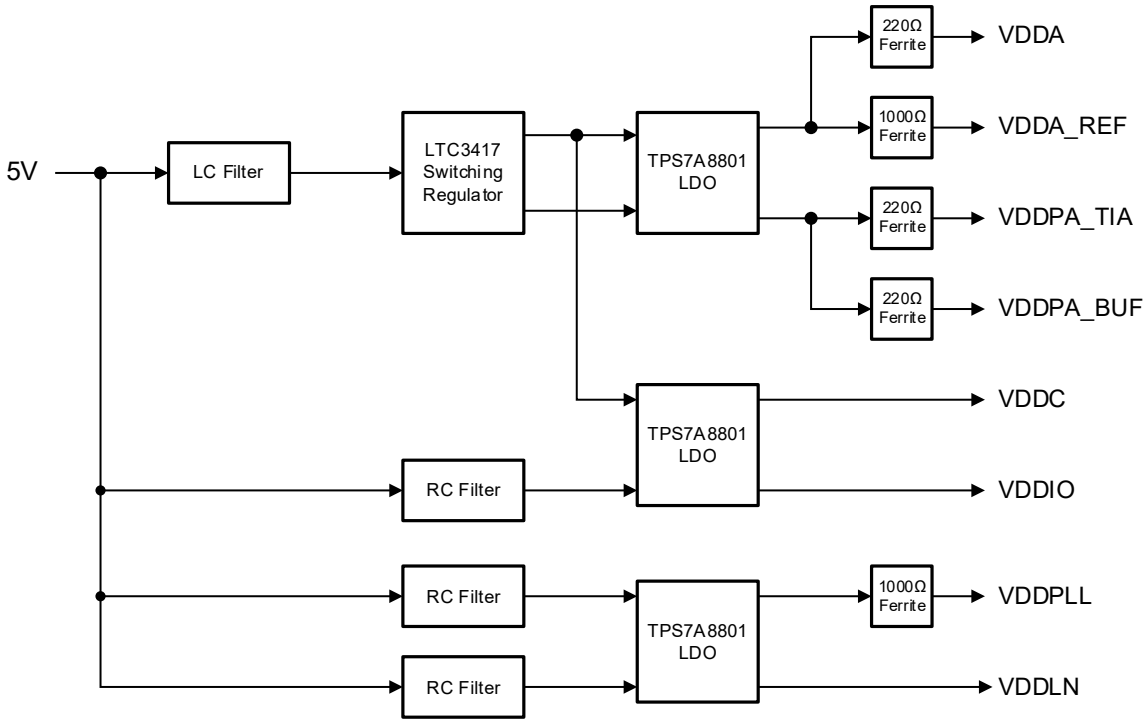


Figure 4 – LCA2-3DF Evaluation Kit power supply block diagram

Linear Voltage Regulators

To achieve the noise requirements for the LCA2, the use of low-noise linear voltage regulators (LDOs) is mandatory. The designer should refer to the LCA2 LeddarCore Data Sheet for noise specifications to be considered when designing a power supply for the LCA2.

By way of example, the LCA2-3DF Evaluation Kit uses the TPS7A8801 from Texas Instruments®, which is a dual LDO with low-noise performance.

Switching Voltage Pre-Regulator (Optional)

Linear voltage regulators are suitable to achieve low-noise performance as well as a high PSRR (power supply rejection ratio). However, they can be inefficient and dissipate a substantial amount of heat if the voltage drop across them is too high. The power dissipated by a linear regulator is given by the following relationship:

$P_{LOSS} = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} I_Q$, where I_Q is the quiescent current required by the LDO for its internal circuitry.

In most cases, one cannot reduce the amount of current going through a given rail, as it is dictated by the application. However, the voltage drop across the voltage regulation can be reduced by employing a switching pre-regulator. Switching regulators can be much more efficient than linear regulators (>90% is not uncommon). The downside of using switching regulators is that their noise performance is sub-par when compared with their linear counterparts. Using a switching pre-regulator followed by linear regulators permits to leverage the best of both types of regulators. The result is a power supply design that is both efficient and low-noise, at the expense of added complexity and cost.

On the LCA2-3DF Evaluation Kit, a dual synchronous step-down DC/DC regulator was used, namely the LTC3417 from Linear Technology®.

Filtering and Decoupling

Each power supply rail should be filtered with an inductor and capacitors. Every supply pin should have a 470 pF capacitor in parallel with a 100 nF capacitor directly connected to the supply pin. The capacitors should be of the X7R ceramic type or C0G rating. Additionally, a 10 µF tantalum or ceramic capacitor should be used for each rail. Figure 5 illustrates an example of decoupling used on the LCA2-3DF Evaluation Kit.

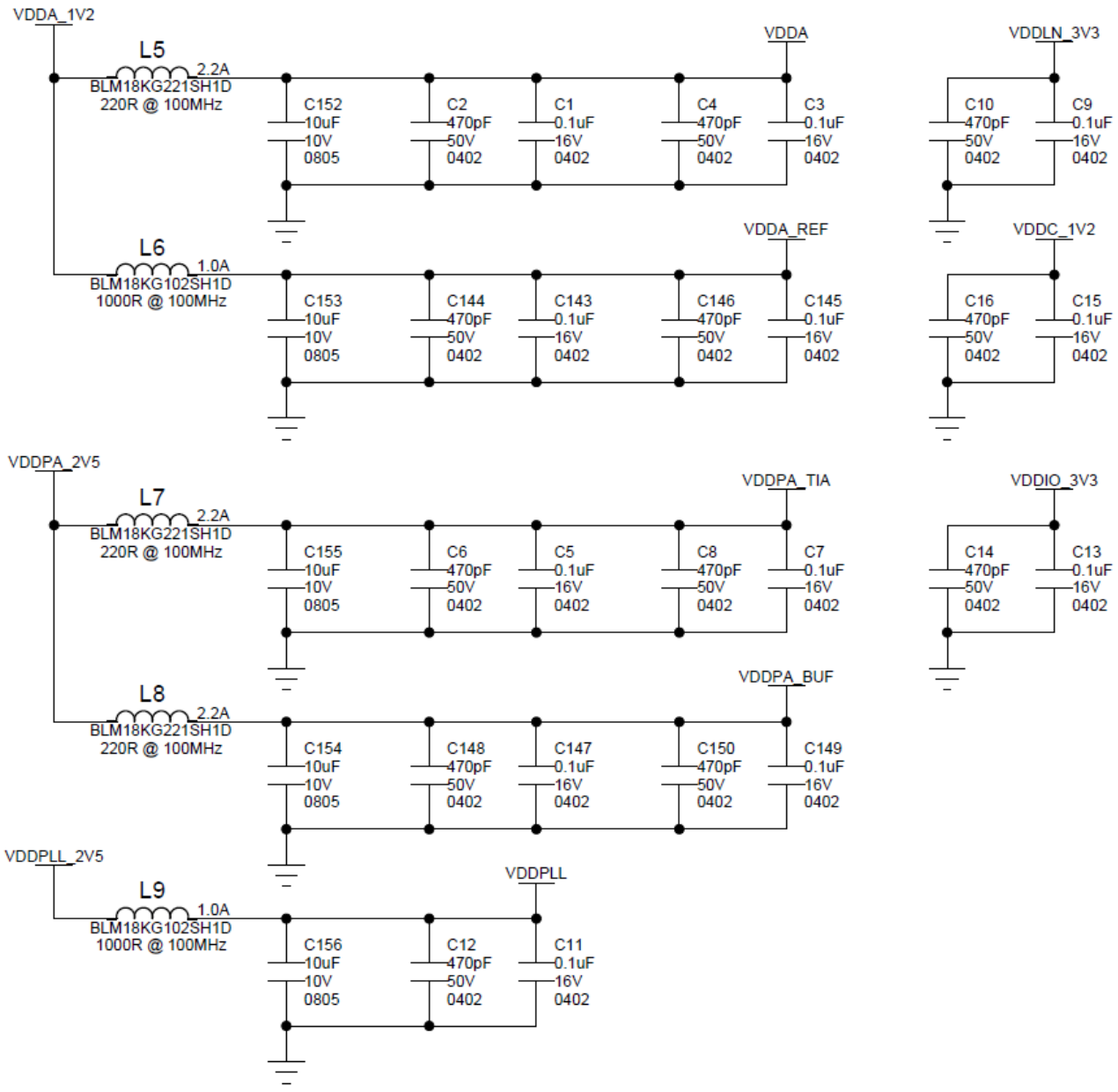


Figure 5 – Example of decoupling used on the LCA2-3DF Evaluation Kit

Reset and Clock

Although the reset and reference clock signals do not directly fall under the scope of this Developer Guide, they have timing requirements with respect to the power supply sequencing that must be considered. It is, therefore, recommended that they be managed and implemented in accordance with the power supply rails.

Furthermore, to ensure the proper functioning of the LeddarCore SoC, noteworthy is that the oscillator clock must not be operating before all the supply rails have come up. The solutions outlined in this Developer Guide can be adapted to take this into account. For example, if using a microcontroller to do the power sequencing, it is easy to

add an output for the reset signal and another one for the oscillator enable signal. Their timing can then be controlled in relation to the other power supply strobes.

Conclusion

This Developer Guide highlighted the power requirements for the LCA2 LeddarCore SoC. Furthermore, the requirements in terms of power supply sequencing and noise were also addressed. Finally, this document outlined the implementation details and recommendations about power supply design for the LCA2.

References

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5. Walt Kester, James Bryant, and Mike Byrne, “Grounding Data Converters and Solving the Mystery of AGND and DGND,” Analog Devices, MT-031

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6. Enger, Nathan, “Power Supply Sequencing Simplified,” Analog Devices, Design Note 1037

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This Developer Guide does not constitute a reference design. The recommendations contained herein are provided “as is” and do not constitute a guarantee of completeness or correctness.

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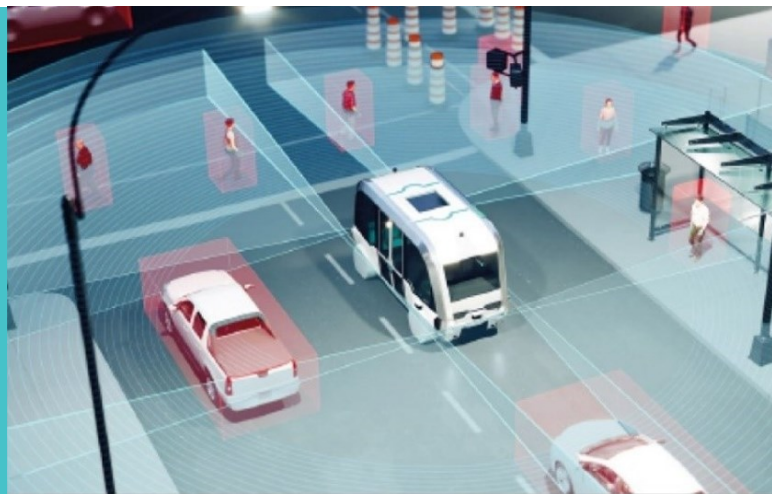

LeddarTech®

CANADA – USA – AUSTRIA – FRANCE – GERMANY – ITALY – ISRAEL – HONG KONG – CHINA

Head Office
4535, boulevard Wilfrid-Hamel, Suite 240
Québec (Québec) G1P 2J7, Canada
leddartech.com

Phone: + 1-418-653-9000
Toll-free: 1-855-865-9900